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JUN 0 9 2004
PATENT & TRADEMARK OFFICE

Docket No.: 57454-970 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Hideto HIDAKA	:	Confirmation Number: 7630
Serial No.: 10/644,750	:	Group Art Unit: 2818
	:	Allowed: May 24, 2004
Filed: August 21, 2003	:	Examiner: Yoha, Connie C.

For: MIS SEMICONDUCTOR DEVICE HAVING IMPROVED GATE INSULATING FILM RELIABILITY

REQUEST FOR ACKNOWLEDGEMENT OF THE "CORRECTED" CITED ART

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We are in receipt of the Notice of Allowance dated May 24, 2004.

It is noted that the Examiner has not initialed a copy of the corrected PTO-1449 that accompanied the Supplemental Information Disclosure Statement filed March 17, 2004. The Examiner initialed and returned PTO-1449, filed August 21, 2003, which contained an inverted reference number. The Supplemental IDS filed March 17, 2004 corrected this typographical error. A copy of the corrected 1449 is attached and for the Examiner's convenience, the corrected reference is highlighted. It is respectfully requested that the Examiner initial the pto-1449 and provide applicants with an initialed copy thereof.

It is respectfully requested that the records of the Patent Office be corrected to ensure that the deed of Letters Patent will be printed correctly.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

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Date: June 9, 2004

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JC177

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
57454-970	**No. 10/644,750**
APPLICANT: **Hideto HIDAKA**	
FILING DATE: **August 21, 2003**	GROUP: **2818**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US	6,414,889	07/2002	Chen et al.	
		US	6,107,134	08/2000	Lu et al.	
		US	5,956,279	09/1999	Mo et al.	
		US	5,694,364	12/1997	Morishita et al.	
		US	5,379,260	01/1995	McClure	
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
		"A Precise On-Chip Voltage Generator for a Gigascale DRAM with a Negative Word-Line Scheme", by Tanaka et al., IEEE Journal of Solid-State Circuits, Vol. 34, No. 8, 8/1999, pp. 1084-1090.	
		"Ultra LSI Memory" by Kiyoo Ito, Advanced Electronics Series, November 5, 1994, published by Baifukan, pp. 351-371.	
		"An Experimental 256-Mb DRAM with Boosted Sense-Ground Scheme", by Asakura et al., IEEE Journal of Solid-State Circuits, Vol. 29, No. 11, 11/1994, pp. 1303-1309.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.